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# Effect of phonon confinement on heat dissipation in ridges

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***Abstract-* We have investigated experimentally the effect of lateral confinement of acoustic phonons in ridges as a function of the temperature. Electrical methods are used to generate phonons in 100nm large nanostructures and to probe the nanostructure temperature in the same time, what allows tracking the heat flux generated and its possible deviation from Fourier diffusive heat conduction. We compare our results with those of a recent theoretical paper based on the ballistic-diffusive equations.**

## I. Introduction and Background

Heat transfer in non-metallic materials is mediated mainly by phonons. Even in highly-doped silicon indeed, the electronic contributions to the thermal conductivity $\lambda$ stays very small: One can show with the Wiedemann-Franz law that for an electrical resistivity of $\rho = 10^{-5}$ $\Omega$.m the electronic thermal conductivity is lower than 1% of the phononic one. In large systems and devices phonon heat transfer is determined basically by the material properties. But state-of-the-art microelectronic devices reach routinely dimensions in the sub-100 nm regime, where confinement effects play a significant role. At this scale, the heat transfer does not depend only on the material bulk properties. Numerous works have recently showed the decrease of the effective thermal conductivity in materials due to phonon confinement. It has been demonstrated in particular in thin layers [1], in nanowires [2,3,4] or in polycrystalline materials with nanometre-scales grains [5]. In order to recall the pertinent sizes, we have plotted the two characteristic sizes of the phononic transfer, the phonon mean free path linked to the quasi-particle behaviour and the phonon wavelength linked to the wave one, as a function of the temperature (see Figure 1). One needs to keep in mind that these are mean values and that in reality they span around these averages on quite large "spectra". In the case of the wavelength, it is related to the Bose-Einstein distribution and one can define a kind of Planck spectrum for phonons. In the case of the mean free path the spectrum is much less known. It appears therefore very useful to probe regimes where the mean free path will be of the same order than the critical device dimension. The ratio of the averaged mean free path to the device size defines the Knudsen number $Kn=\Lambda/D$ of the heat transfer that can quantify the transition between the diffusive to the ballistic regime.

In this work, we use the temperature as a parameter to probe different ranges of Knudsen numbers. We report on the investigation of the heat transport from silicon ridges into bulk Si substrates (see Figure 2).

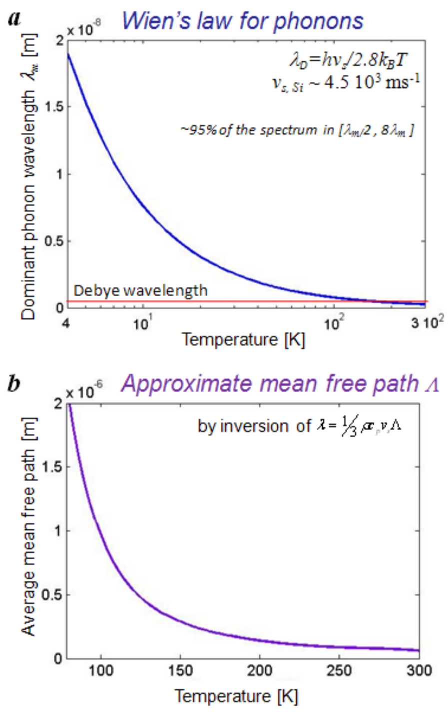


Fig. 1a. Dominant phonon wavelength $\lambda_m$ as a function of the temperature. Note that near room temperature the Debye cut-off will modify the shape of the Planck spectrum. Fig 1b. Approximate mean free path $\Lambda$ as a function of the temperature. It is obtained by inverting the expression of the thermal conductivity. Note that this clearly overestimates the contribution of the optical phonons and therefore minors the real average mean free path.

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## II. Samples Fabrication

Our aim is to investigate interesting geometries such as the ridge one shown on Figure 2. We fabricated samples made of electric conductors (also called heaters in the following) on top of silicon ridges. These ridges stand on a planar Si wafer. The goal is to generate a heat flux in the conductor through means of Joule dissipation and to monitor how well the heat flux is transferred to the substrate.

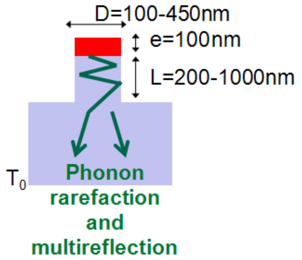


Fig. 2. Geometry of the probed devices: a heater (in red) stands on top of a high ohmic Si ridge (in blue) which lays on a planar substrate.

In order to prepare such samples, different paths have been envisaged. We fabricated three types of devices, which utilize different heater layers (red in Figure 2): a $n^+$ Si heater with implanted donors, an epitaxial $n^+$ Si heater, and a metal heater. The main advantage of the $n^+$ Si heaters in comparison to the metallic one is that they do not introduce any additional material interface that can lead to a large thermal boundary resistance between the metal and the Si ridge. The implanted heater has a doping concentration gradient (due to the implantation process and subsequent annealing) while the epitaxially grown sample has a sharp step-like doping profile at the interface between the epitaxial layer and the silicon. The latter is therefore more suitable for the interpretation of the experiments. In the following, the heat transport properties reported are based on samples with 100 nm-thick epitaxial $n^+$ Si heater layer grown on high ohmic silicon substrate. The $n^+$ epitaxial layer contains a density of $5\times10^{19}$ $cm^{-3}$ of phosphorous atoms, which is sufficient to make of Si a degenerate system with metallic behaviour.

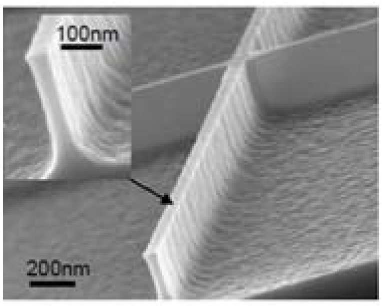


Fig. 4. SEM images of the ridges on top of the samples. One observes in the insert that the profile at the bottom of the ridge is not perfectly sharp. The remaining roughness can be estimated to be around 10 nm.

The ridges and the $n^+$ heater were patterned with electron beam lithography and inductively-coupled plasma (ICP) etching. We used the high-resolution negative tone electron beam resist HSQ. During the exposure this resist is converted into $SiO_2$-like material, presenting a good mask with high resistivity to the plasma etching. This $SiO_2$ layer served as an etching mask against the $C_4F_8$/ $SF_6/O_2$ plasma of the ICP etcher. The ridge height was controlled with the ICP etching time. Figure 4 shows SEM images of cleaved test structures. The ridge edge exhibits surface roughness of ~ 10 nm. The shapes of the structures reported further are summarized on Figure 5. We have kept the heater thickness and modified the ridge width and thickness. The heater width is the same as the ridge's one.

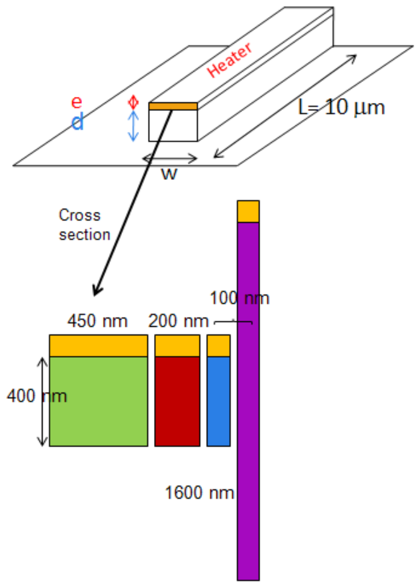


Fig. 5. Schematic of the cross sections of the investigated structures. The heater thickness (here in yellow) is 100 nm.

## III. Measurement Setup

The measurement of the thermal conductance to the substrate is derived from the $n^+$ epitaxial Si heater temperature, which is acting in the same time as the heat dissipater and a thermometer. The measurement is performed in the standard 4-point geometry (see Figure 6). We consider two different ways to measure the temperature of the heater, both being based on the fact that the heater resistivity $\rho$ depends on the temperature:

$$\rho(T) = \rho_0(T)[1+\alpha\Delta T],$$

where $\rho$ is the electrical resistivity at the reference temperature and $\alpha$ is the temperature coefficient, which describes the change in the resistivity due to small temperature change $\Delta T << T$. Note that $\alpha$ depends on the temperature and cannot be considered constant over the full range of temperature measurement.

The first type of envisaged measurement is based on the technique known as the 3ω method [6]. By using a sine current $I=I_\omega \cos \omega t$ as input in the heater, we generate a temperature field that possesses a DC component and also a 2ω one due to the Joule effect ($T=T_0+T_{DC}+T_{2\omega} \cos (2\omega t+\phi_{2\omega})$ ). The voltage of the heater therefore possesses a 3ω harmonic component due to the temperature-dependent electrical resistance. The interest lies in the linear

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dependence of this harmonic to the 2ω temperature. One reads

$$V = V_\omega + R_0 I_\omega \alpha T_{2\omega}/2 \cos(3\omega t+\phi_{2\omega}),$$

where $\phi_{2\omega}$ is the phase between the input current and the temperature field at 2ω. Note that here $T_{2w}$ is the integration of the temperature over the wire.

The other method to measure the temperature is based on a DC heating and the measurement of the resistance with the help of a very low AC sine current. By neglecting the heating due to the harmonic current, one can perform a differential measurement of the temperature. Indeed, the voltage of the heater then reads

$$V = V_0 + R_0 (1+\alpha T_{DC}) I_\omega \cos \omega t,$$

where $T_{DC}$ can be retrieved by subtracting the voltage measured without DC excitation. Note that both techniques require lock-in detection of the voltage at 3ω and 1ω respectively. In the following we report only results found with the second technique, which proved more suitable for our samples.

The heat transport measurements were performed in an open cycle nitrogen filled cryostat. The substrate temperature of the devices was set and controlled by the nitrogen flow and with the help of a heater located in the cryostat. The substrate temperature was given by a calibrated diode thermometer located on the sample holder. Each ridge heater was calibrated at low-power excitation by measuring its electrical resistance as a function of the substrate temperature. At room temperature, the sheet resistance of the $n^+$ layer is 130 Ω and the temperature coefficient α is positive. On average in the experimental temperature range we have $\alpha \sim 1.5\times10^{-3}$K$^{-1}$.

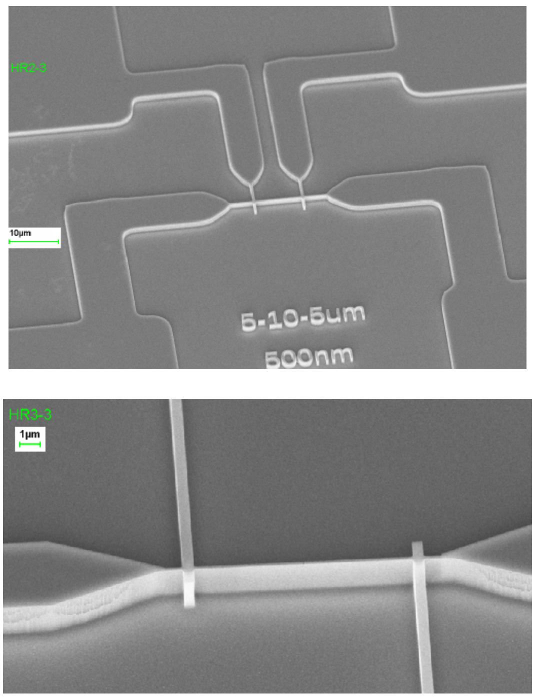


Fig. 6. Two examples of measured 4-points devices which are 10 micrometers long. The heater and the silicon ridge are indiscernible on both SEM micrographs.

## IV. Measurement Results

Measurements were performed on four devices with epitaxial heater and with the superimposed AC-DC method (the dimensions are illustrated in Fig. 5). Knowing the average temperature of the device and neglecting the radiation losses, we are able to trace back the heat flux transferred to the sample and the thermal conductance of interest. In the following, we neglect the heat flux lost in the 4 arms (see Fig. 6) of the devices. Therefore, our results essentially represent an upper limit of thermal conductance. Finite element simulations of the devices have shown that metallic microscale 3ω devices lose no more than 12% of the heat flux through the contacts [7]. In sub-micron devices like those considered here, this effect should be even smaller. Note also that the highly-doped silicon has a lower thermal conductivity than the undoped Si substrate due to increased phonon scattering, which also supports our approximation.

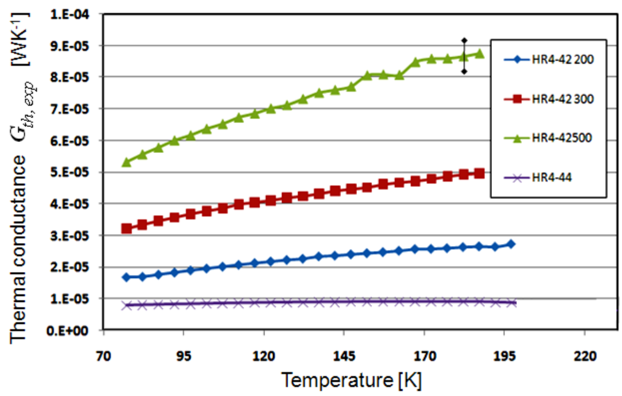


Fig. 7. Measured thermal conductances $G_{th\ exp}$ as a function of the temperature for the 4 devices sketched higher (the colors are the same).

Figure 7 shows the experimental thermal conductance of the four ridge devices as a function of the temperature. For the three devices that possess the same height, we observe a consistent decrease of the thermal conductance when decreasing the device width. The much taller device shows a smaller thermal conductance.

## V. Comparison with Fourier Heat Transfer

We calculate theoretically the thermal conductance that we would find in the case of Fourier's heat transfer when using the bulk silicon thermal conductivity [8] ($\lambda_{Si}$=149 Wm$^{-1}$K$^{-1}$ at room temperature). The heat path can be divided in two parts, a standard 1D flux in the vertical direction (1) followed by a zone of expansion of the heat flux lines (2) in the substrate. These thermal resistances (1) and (2) are in series. We therefore sum them: $R_{th\,F}=R_{th\,F\,1}+R_{th\,F\,2}$. (1) is trivial but the calculation of (2) has to be done according to Yovanovich's work [9].


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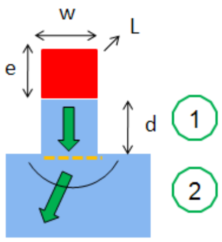


Fig. 8. Heat path after generation in the heater (red):
1D flow (1) followed by the expansion of the heat flux lines (2).

A difficulty lays in the description of the heat flux lines near the connections of the ridge with the contacts. We cannot do better than simply neglecting the perturbation due to the ends. It is difficult to quantify this effect, but it is to be noted that this has always been neglected in the work with micrometer-scale 3ω devices. Note that we calculate the thermal resistance (2) in the 3D configuration in addition to the usual 2D infinite wire case generally adopted. We keep the 3D results, but present in Table I both types of results for the sake of comparison.

TABLE I

Thermal resistances $R_{th\,F\,2}$ and associated conductances for the geometries of different devices calculated in the 2D and 3D cases, given in $KW^{-1}$ (resp. $WK^{-1}$).

| Device | | | 2D (adiabatic boundaries) | | 3D | |
|---|---|---|---|---|---|---|
| | Length L | Width w | $R_{th}$ | $G_{th}$ | $R_{th}$ | $G_{th}$ |
| HR4_42_200 | 10 µm | 100 nm | $2.512\ 10^{5}/\lambda$ | $3.98\ 10^{-6}\ \lambda$ | $1.99\ 10^{5}/\lambda$ | $5.03\ 10^{-6}\ \lambda$ |
| HR4_42_300 | 10 µm | 200 nm | $2.512\ 10^{5}/\lambda$ | $3.98\ 0^{-6}\ \lambda$ | $1.67\ 10^{5}/\lambda$ | $5.99\ 10^{-6}\ \lambda$ |
| HR4_42_500 | 10 µm | 450 nm | $2.512\ 10^{5}/\lambda$ | $3.98\ 10^{-6}\ \lambda$ | $1.37\ 10^{5}/\lambda$ | $7.27\ 10^{-6}\ \lambda$ |
| HR4_44_200 | 10 µm | 100 nm | $2.512\ 10^{5}/\lambda$ | $3.98\ 10^{-6}\ \lambda$ | $1.99\ 10^{5}/\lambda$ | $5.03\ 10^{-6}\ \lambda$ |

We observe a linear (respectively an inverse linear) dependence of the thermal conductance (respect. resistance) (2) to the thermal conductivity. Taking into account (1) and (2) in Table I allows us to plot the measured thermal conductances $G_{th\ exp}$ normalized by Fourier's ones $G_{th\,F} = 1/R_{th\,F}$ in Figure 9.

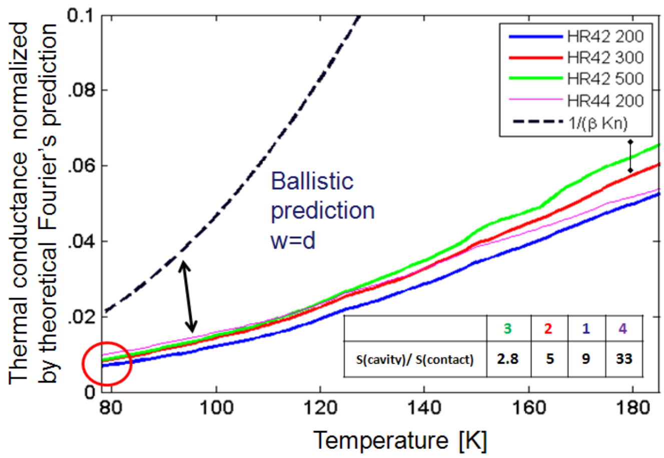


Fig. 9. Thermal conductances of Fig. 7 normalized by Fourier's results $G_{th\,F}$ calculated following Yovanovich as a function of the temperature. The dotted line is a guide for the eyes representing the pure ballistic prediction in the case w=d. The table insert shows the ratio of the heater cavity surface to the constriction area.

The first result is that we confirm that we are far from Fourier's regime ($Kn \rightarrow 0$). Indeed, the normalization shows that the heat transport is much less efficient than what implies the classic heat equation: Less than 10% in the full temperature range and as low as 1%. Note that we are here in a broad range near $Kn$=1 (see Figure 1) and that we are still at larger scale than where wave effects affect the heat transport. The order found in Figure 7 is confirmed, apart from the violet curve which now crosses the other curves.

## VI. Comparison with the Ballistic Regime

The heat transfer through a constriction can be calculated in the case of the ballistic regime, when $Kn \rightarrow +\infty$. This happens when the constriction dimension becomes much smaller than the phonon mean free path. In this regime the thermal conductance becomes independent of the mean free path of the unconfined bulk material; the mean free path can be replaced by the characteristic size of the device, which is now the smaller size representing the free flight of a phonon without collision. By analogy with electronics, one can write the so-called Sharvin term as follows:

$$R_S = \frac{3\beta}{c_p v_s w^2},$$

where $\beta$ is a geometric factor depending of the geometry of the contact, $c_p$ the specific heat, $v_s$ the sound velocity and $w$ the width. Note again that this is an approximated expression as it overestimates the contribution of the optical phonons.

In principle, the thermal resistances in the transition regime (Kn~1) between Fourier's one and the ballistic one have to be calculated according to the Boltzmann transport equation (BTE), which describes the phonon evolution at each frequency. A very common approximation is to use the sum of the Fourier term (also called Maxwell constriction term $R_M$ for historical reasons) and the ballistic (Sharvin) one $Rs$:

$$R_W = R_M + R_S$$

This is the Wexler approximation [10]. The idea is that in both regimes the corresponding term is leading and that in the transition regime the sum is not too far from the exact result. This has indeed been verified in electronics for the case of a round constriction between two heat baths [11]. Note that it is also possible to write the Wexler approximation as

$$R_W = R_M (1 + \beta.Kn).$$

In Figure 9, we also plotted the normalized ballistic approximation (black dotted line) $1/(\beta\,Kn)$ for the case w=d (squared shape of the ridge cavity) where β=2.24. We consider pure ballistic transmission in the ridge for this normalization and assume that $R_{th\,ball} = R_W$ by neglecting the effect of the ridge. The very striking result is the large difference between the ballistic prediction and our measurement, which is much larger than the maximum difference of 11% found in Ref. [11].


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## VII. Discussion

There are two phenomena that have to be discussed: *(A)* The large difference with the ballistic and Fourier regimes and *(B)* the thermal conductance behavior of the high aspect ratio ridge (violet curve in Figure 7 and 9).

### A. *The large difference with the ballistic and Fourier predictions*

The main difference between our geometry and the previously analyzed ones is that we do not have two large heat baths at the sides of the constriction. A phonon coming from the cold substrate and entering into the heater can be reflected by the heater boundaries to the cold substrate without thermalizing in the heater cavity. Indeed, the thermalization would require numerous interactions with the heater phonon bath, which do not happen due to its nanometer-scale size (even the heater boundaries and inner part are not thermalized). It has been recently proposed theoretically [12] that this effect might be responsible for an increase of the thermal resistance between a nanostructure and a thermal bath. This is exactly the geometry we have investigated experimentally in this paper.

The ability for a phonon to thermalize by the cavity when impinging on it coming from the substrate depends grossly on the ratio of the cavity surface to the constriction surface. The table inserted in Figure 9 gives these ratios. One can observe that it indeed provides scaling for the d=400 nm curves: The larger the ratio the larger the thermal resistance.

As presented in Ref. [12], the total thermal resistance can be written

$$R_{th} = R_M(1+\beta Kn).C(W/BTE)\frac{1}{1-\gamma}$$

where *C(W/BTE)* is the BTE correction to the Wexler approximation and the $\gamma$ term responsible for the correction to the "two heat baths" case when a nanostructure is involved. Unfortunately, in the case of the squared wire shape deposited on the surface there is no calculation of *C(W/BTE)* available in order to compare exactly the thermal resistance measured with the prediction. However, one can observe in Ref. [12] that this term can reach ~5 for the case of a vertical cylinder with aspect ratio of 1. This is similar to what we observe in Fig. 9.

### B. *The different behavior of the high aspect ratio ridge*

The behavior of the normalized thermal conductance as a function of the temperature (violet curve) representing the evolution of the ridge with high aspect ratio (d=1.6 μm) appears to be very different from the three different ones when normalized by the Fourier thermal resistance. While the order is conserved through the full range of Knudsen number for the three d=400 nm curves, it is not the case for this one. We observe that at the lowest temperature the thermal conductance is the highest one of our devices whereas at the highest temperature it shows a trend toward the lowest one. The main difference between this device and the others is its huge aspect ratio. Indeed, this sample actually resembles a film anchored to the substrate at one end. In a thin film the effective phonon mean free path is limited by the film thickness. Now, if we assume that the measured thermal resistance is mostly determined by this vertical film and defines the thermal conductance $G_{th\ 1=}\ wL\ \lambda_{filn}/d$ we find that $\lambda_{filn}$ grows from ~11 $Wm^{-1}K^{-1}$ to ~13 $Wm^{-1}K^{-1}$ in our temperature range. This thermal conductivity value is roughly factor of 8 smaller than the one measured from a 100 nm-thick single crystalline (atomically smooth) Si film [13]. The discrepancy can be due on the one hand to the fact that this analysis for $\lambda_{filn}$ ignores the ridge-to-substrate thermal resistance (2) and on the other hand that the ridge edges have relatively large roughness (see Figure 4) which tends to reduce $\lambda_{filn}$.

### C. *Other remaining questions*

The other remaining questions that need to be analyzed in further details are: (a) Is there a significant thermal surface resistance between the doped layer and the silicon? (b) Is there some phonon impedance adaptation at the bottom of the ridge? (c) What are exactly the losses through the contacts? Note that as we have ignored these losses and that the experimental thermal conductances we have shown here present the upper limit values.

## VIII. Conclusions and Perspectives

We have investigated heat transfer between nanostructured ridges of different sizes and a planar substrate as a function of temperature. The temperature and device sizes provide degrees of freedom that allow us to probe a range of phonon Knudsen numbers. The "heater on a ridge" geometry is original as it sets very dissimilar ways for the hot and cold phonon paths. We have presented results in Knudsen regimes far from Fourier heat transfer or ballistic phonon transport. We explain this set of experimental results by observing that we are probing geometries where one cannot consider having two heat baths like what is generally done.

In order to improve our knowledge of the effect, we will now try to investigate other materials as well as to confirm the case of the unconventional aspect ratio. A goal is also to further reduce the dimensions in order to probe wave effects.

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